ATA PC Card (PCMCIA)
Specifications
and
Drawings

32MB to 4GB ATA PC Card (PCMCIA)

ORDERING INFORMATION

GalaxyStor P/N	Capacity
GE2PCTI032(x)*	32 Mbytes
GE2PCTI064(x)*	64 Mbytes
GE2PCTI128(x)*	128 Mbytes
GE2PCTI256(x)*	256 Mbytes
GE2PCTI512(x)*	512 Mbytes
GE2PCTI1GB(x)*	1.0 Gbytes
GE2PCTI2GB(x)*	2.0 Gbytes
GE2PCTI4GB(x)*	4.0 Gbytes

All GalaxyStor Solid State Drives are built to our Enhanced Industrial Operating Temperature range option.

*** A = Part Number Listed on Card Label**
B = Part Number and Serial Number listed on Card Label

FEATURES

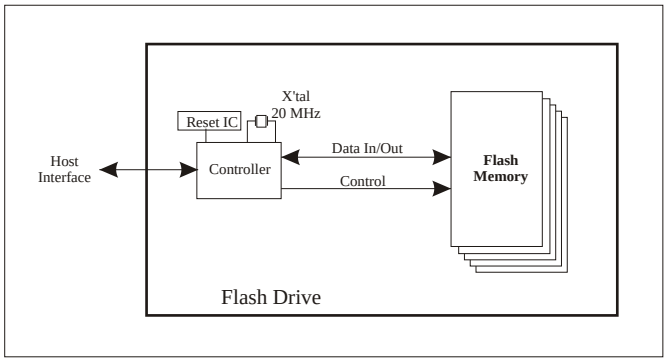
- Capacities from 32MB to 4.0GB.
- Standard Type I PC Card Form Factor.
- PC Card Standard Release 8 Compliant.
- CIS (Card Information Structure) programmed into 256 Bytes of Attribute Memory.
- Low Power Dissipation
  - High Performance Read Current: 55mA @ 5V, 40mA @ 3.3V
  - High Performance Write Current: 55mA @ 5V, 40mA @ 3.3V
  - Sleep Mode: 200uA
- Supports both PC Card ATA and True IDE Interface Modes
- Enhanced Industrial Operating Temperature Range from -40 to +100 Degrees Celsius

GENERAL DESCRIPTION

The GalaxyStor GEPCTI Series PCMCIA Card are solid-state PC Cards with capacities of 32MB to 4.0GB with a standard PCMCIA Type I form factor.

The PC Cards use a flash memory controller that provides for a fully compatible PC Card ATA interface for the flash memory. This allows the use of the lightweight, low-power, and rugged flash memory for removable mass storage.

FUNCTIONAL BLOCK DIAGRAM



General Description

The GalaxyStor GE2PCTI Series PCMCIA Cards are OEM Grade PC Cards, (also referred to as Industrial Grade). GalaxyStor does not design or build it's Solid State Product for Retail use so the customer is always assured of high quality product for use in their required applications. The PC cards are available with 32MB to 4.0GB of non-volatile Storage.

The GE2PCTI Series cards are Type I Form Factor PC Cards and available in Enhanced Industrial temperature range only. The GE2PCTI Series PC cards use a Lexar Brand intelligent flash memory controller that provides for a fully compatible PCMCIA interface for the NAND flash memory. The on-board controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control for the entire Card. The proprietary space manager architecture in the controller maximizes read/write data rate performance to and from the host and flash memory, eliminating firmware delays during sector read and write operations. The Lexar controller, combined with tailored firmware, provides complete ATA disk emulation, which ensures full compatibility with a wide range of operating systems (ideal for mobile computing devices, professional digital photography, and most commercial applications using Solid State Devices).

The on-board controller contains many capabilities not found in many standard memory devices.
These functions include, but are not limited to:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Host independence from details of erasing and programming flash memory.
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives).
- Sophisticated system for error recovery including a powerful error correction code (ECC).
- Power management for low power operation.

Some benefits of solid state over rotating media are higher shock resistance, no moving parts, more tolerant under harsh operating conditions, no noise, low profile, low power, etc.

The host side of the card is standard PCMCIA interface with IDE/ATA support as per CF and PCMCIA specifications. The 512-byte sector size of the OEM PC Card is the same as that in an IDE rotating disk drive. To write or read a sector (or multiple sectors), the host simply issues a Read or Write command, which contains the address and the number of sectors to write/read, to the card. The host then waits for the command to complete. The host is not involved in the details of how the flash memory is erased, programmed or read. Because of this, the host system software will not require changing as new flash cards evolve (Faster speeds and higher capapcities) and systems that support the OEM PC Card today will be able to access future GalaxyStor cards built with new flash technology without having to update or change host software. All GalaxyStor PC Cards are compatible with standard software such as Microsoft Windows versions, Linux, and embedded software. This software compatibility includes initializing the PC cards and using standard ATA drivers.

GalaxyStor OEM PC Cards contain a sophisticated defect and error management system which is completely transparent to the host and does not consume any user data space. The soft error rate for OEM PC Cards is much lower than the rotating disk drive specification and the card has innovative algorithms to recover data in the rare case a read error would occur. These defect and error management systems, coupled with the solid-state construction, give GalaxyStor OEM PC Cards exceptional reliability.

Another feature of the GalaxyStor PC Card is it's automatic entrance and exit from sleep mode. Upon completion of a command, the card will enter sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur. In most systems, the card is in sleep mode except when the host is accessing it, thus conserving power. When the host is ready to access the card and it is in sleep mode, any command issued to the card will cause it to exit sleep and respond.

Which methods are employed by the controller to increase its expected life-time?

The PCMCIA controller implements several methods that increase its reliability and expected lifetime.

Natural Wear Leveling

Dynamically and automatically moves the data around the entire media so that each flash block wears out evenly. The controller monitors the internal pointer not to use specific blocks repeatedly. For example, when the data is written to block 1, the controller/firmware first moves the data to the first available block, block 2 and then erases block 1 to mark this block as an empty block. The next time when data is written to block 4, the internal pointer now points to block 5. The controller/firmware moves the data to block 5 and then erases block 4 to mark this block as an empty block. This algorithm ensures that each block is used evenly across the entire Media.

Hardware Error Detection and Correction (EDC/ECC) and Cyclic-Redundancy Code (CRC)

GalaxyStor uses an enhanced 48-bit Reed-Solomon code and CRC that is specifically designed to handle the error characteristic of the Flash technology being used. ECC code consists of 6 bytes per 512 bytes. The ECC code is stored in Flash along with the data during a write operation. Upon being read back, the stored ECC code is compared to the ECC code generated when the data was read. If the codes don't match, they are decrypted to determine which bit in the data is incorrect. The erroneous bit is flipped and the controller releases the corrected data. Errors are corrected on-the fly, resulting with no performance loss. GalaxyStor uses the standard Single Error Correcting, Double Error Detecting Hamming code (SECDED).

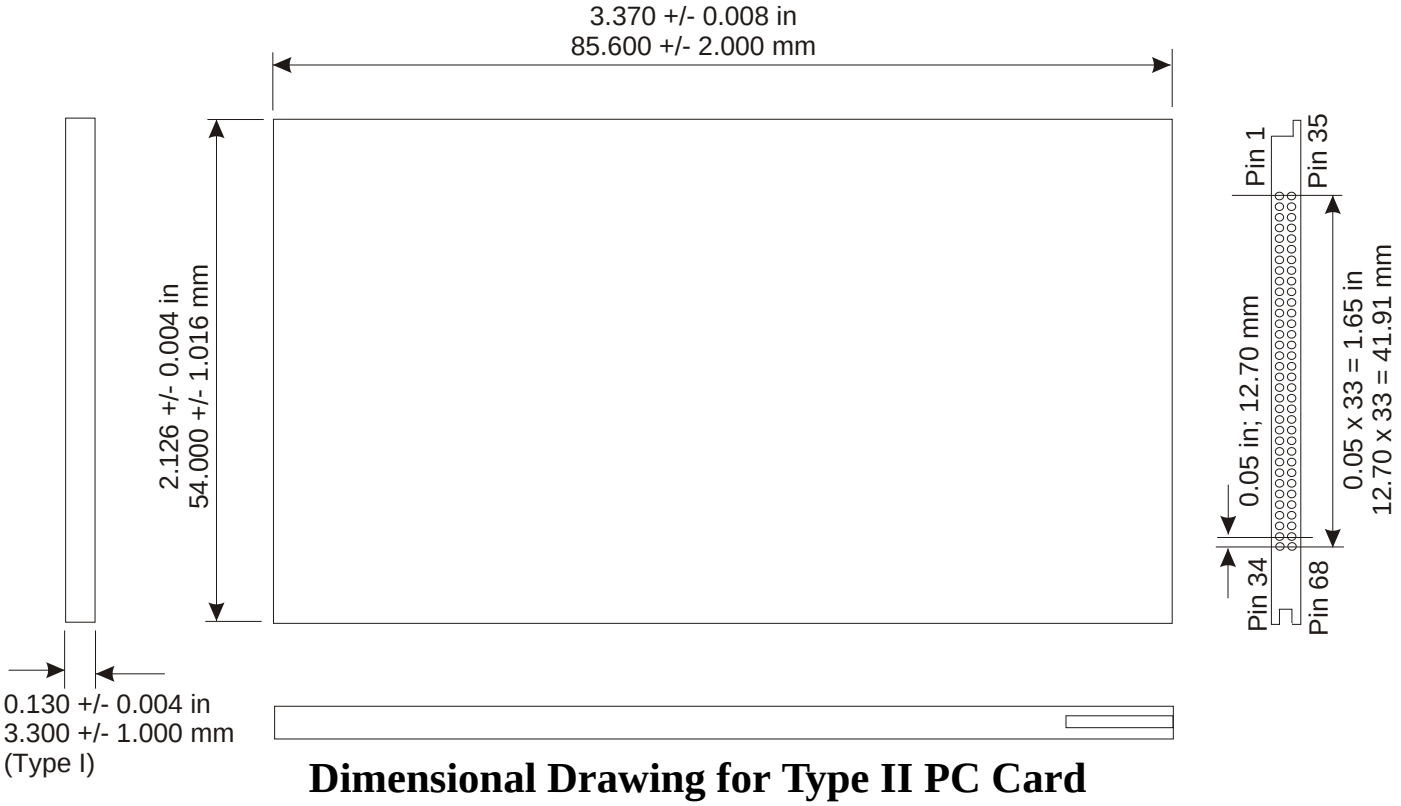
Bad block management

Tests for bad blocks during write and erase and automatically swaps out bad blocks WITHOUT losing any data and performance of good blocks. When the card is formatted, 1 to 1.5% of the media is allocated as spare to handle any bad blocks that might be detected over the years of operation. These units are also cycled by the wear leveling algorithm.
Samsung projects the additional block failure rate at under 0.1% up until 1 million program/erase cycles. By using the standard Single Error Correcting, Double Error Detecting Hamming code, the CF controller can correct one bit reading error per page without replacing any block.

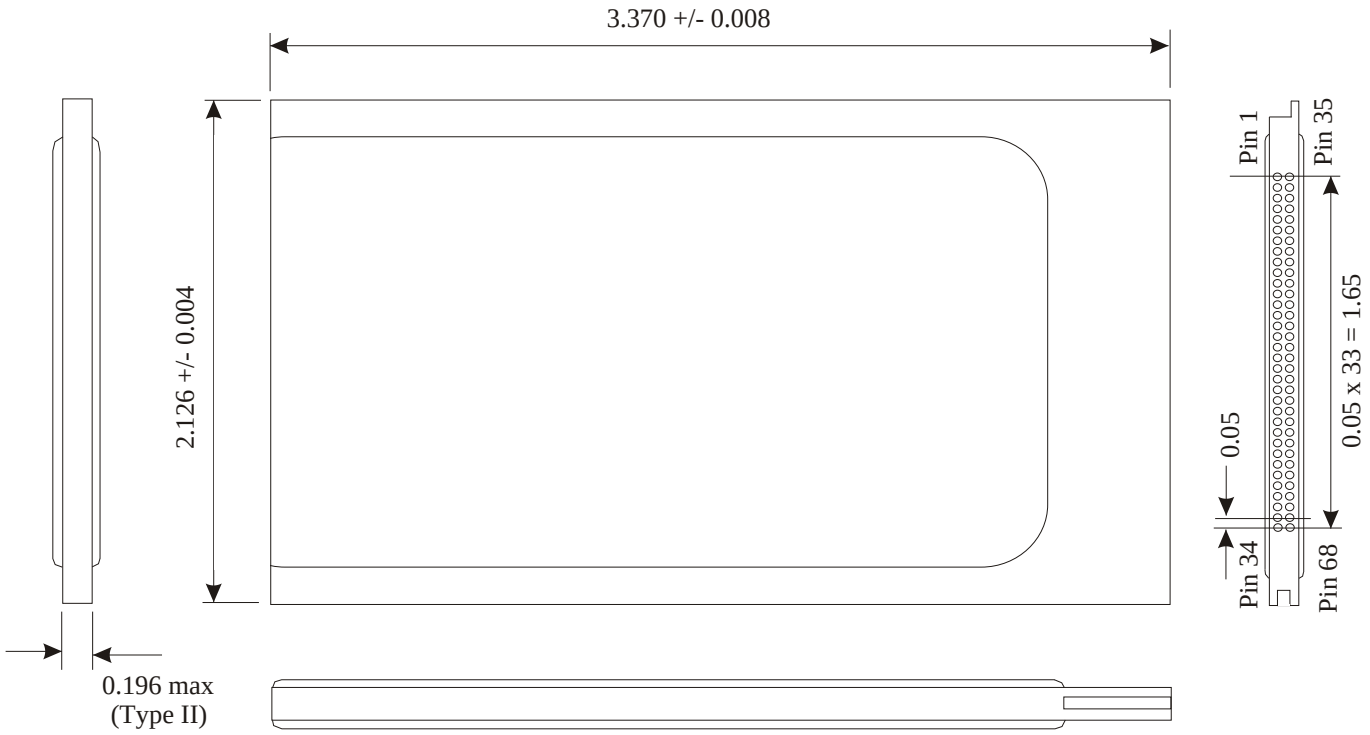
What is the Space Manager Technology?

Unlike magnetic/rotating media in which data can be overwritten, in flash media data must be erased before new data can be written. Direct mapping between logical and physical addresses will require erase-before-write or erase-after-write moves that significantly slow write performance. Other LINK LIST-mapping techniques require large memory space and significant delays in the case of long links. Lexar Media's proprietary-and patented Space Manager technology uses indirect mapping between logical and physical addresses. This allows many sectors to be programmed without any erase Cycles.

Dimensional Drawing for Type I PC Card



Dimensional Drawing for Type II PC Card



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
All input/output voltages	Vin, Vout	-0.5 to VCC +0.5	V	1
VCC voltage	VCC	-0.3 to +6.7	V	
Storage Temperature range	Tstg	-100 to +151	^{o}C	

1. Vin, Vout min=2.0V for pulse width – 20ns

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Enhanced Industrial operating temperature	Ta	-40	-	100	^{o}C
VCC voltage	VCC	4.5 3.0	5.0 3.3	5.5 3.6	V

PERFORMANCE

Item	Performance
Start Up Times (Reset to Ready)	< 10 m/sec
Start Up Times (Sleep to Idle)	2 ms (max)
Data Transfer Burst - To /From Host	up to 16.6 Mbytes / s (burst in PIO4 Mode)
Write Data Tranfer	1 Mbytes / s (Typical)
Controller Overhead (Command to DRQ)	2 ms (max)
Data Transfer Cycle End to Ready (Sector Write)	2 ms (typ)

RELIABILITY

Item	Value
Data Write / Erase Endurance	>300,000 erase/program cycles
Data reliability	1 in 10^{14} bits, read
MTBF	> 1,000,000 Hrs

CAPACITANCE (Ta=25 C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	-	-	15	pF	(Vin=0V)
Output Capacitance	Cout	-	-	15	pF	(Vout=0V)

ENVIRONMENTAL CHARACTERISTICS

Item	Value	Item	Value
Operating Shock1	3000 G max.	Operating Vibration	50 G peak to peak (0.5 sine wave)
Non-operating Shock	3000 G max.	Non-operating Vibration	50 G peak to peak (0.5 sine wave)
Humidity	5% to 96%	Altitude	Up to 80,000 ft.

PIN ASSIGNMENTS

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10	I
9	-OE	I	9	-OE	I	9	-OE	I
10	N/C		10	N/C		10	N/C	
11	A09	I	11	A09	I	11	A09	I
12	A08	I	12	A08	I	12	A08	I
13	N/C		13	N/C		13	N/C	
14	N/C		14	N/C		14	N/C	
15	-WE	I	15	-WE	I	15	-WE	I
16	RDY/BSY	O	16	IREQ	O	16	INTRQ	O
17	VCC	Power	17	VCC	Power	17	VCC	Power
18	N/C		18	N/C		18	N/C	
19	N/C		19	N/C		19	N/C	
20	N/C		20	N/C		20	N/C	
21	N/C		21	N/C		21	N/C	
22	A07	I	22	A07	I	22	A07	I
23	A06	I	23	A06	I	23	A06	I
24	A05	I	24	A05	I	24	A05	I
25	A04	I	25	A04	I	25	A04	I
26	A03	I	26	A03	I	26	A03	I
27	A02	I	27	A02	I	27	A02	I
28	A01	I	28	A01	I	28	A01	I
29	A00	I	29	A00	I	29	A00	I
30	D00	I/O	30	D00	I/O	30	D00	I/O
31	D01	I/O	31	D01	I/O	31	D01	I/O
32	D02	I/O	32	D02	I/O	32	D02	I/O
33	WP	O	33	-IOIS16	O	33	-IOCS16	O
34	GND	Ground	34	GND	Ground	34	GND	Ground
35	GND	Ground	35	GND	Ground	35	GND	Ground
36	-CD1	O	36	-CD1	O	36	-CD1	O
37	D11*	I/O	37	D11*	I/O	37	D11*	I/O
38	D12*	I/O	38	D12*	I/O	38	D12*	I/O
39	D13*	I/O	39	D13*	I/O	39	D13*	I/O
40	D14*	I/O	40	D14*	I/O	40	D14*	I/O

PIN ASSIGNMENTS (Continued)

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type
41	D15*	I/O	41	D15*	I/O	41	D15*	I/O
42	-CE2*	I	42	-CE2*	I	42	-CE2*	I
43	-VS1	O	43	-VS1	O	43	-VS1	O
44	-IORD	I	44	-IORD	I	44	-IORD	I
45	-IOWR	I	45	-IOWR	I	45	-IOWR	I
46	N/C		46	N/C		46	N/C	
47	N/C		47	N/C		47	N/C	
48	N/C		48	N/C		48	N/C	
49	N/C		49	N/C		49	N/C	
50	N/C		50	N/C		50	N/C	
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	N/C		52	N/C		52	N/C	
53	N/C		53	N/C		53	N/C	
54	N/C		54	N/C		54	N/C	
55	N/C		55	N/C		55	N/C	
56	-CSEL	I	56	-CSEL	I	56	-CSEL	I
57	-VS2	O	57	-VS2	O	57	-VS2	O
58	RESET	I	58	RESET	I	58	RESET	I
59	-WAIT	O	59	-WAIT	O	59	-WAIT	O
60	-INPACK	O	60	-INPACK	O	60	-INPACK	O
61	-REG	I	61	-REG	I	61	-REG	I
62	BVD2	I/O	62	-SPKR	I/O	62	-DASP	I/O
63	BVD1	I/O	63	-STSCHG	I/O	63	-PDIAG	I/O
64	D08*	I/O	64	D08*	I/O	64	D08*	I/O
65	D09*	I/O	65	D09*	I/O	65	D09*	I/O
66	D10*	I/O	66	D10*	I/O	66	D10*	I/O
67	-CD2	O	67	-CD2	O	67	-CD2	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

* Signals marked with an asterisk are required for 16-bit access, not required when installed in 8-bit systems.

SIGNAL DESCRIPTIONS

Signal Name	Dir	Pin	Description
BVD2 (PC Card Memory Mode)	I/O	62 TTL I/O 300mA Output 100K Pull-Up	This output line is always driven to a high state in Memory Mode since a battery is not required for this product
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product produces no audio.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master / Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	36, 67	These Card Detect pins are connected to ground on the Card. They are used by the host to determine that the Card is fully inserted into the socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
D15-D00 (PC Card Memory Mode)	I/O	37, 38, 39, 40, 41, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30 TTL I/O 3mA Output	These lines carry the Data, Commands, and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15-D00 (PC Card I/O Mode)			This is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode)	I	45	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)		TTL Schmitt Trigger Input 100K Pull-Up	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Card controller registers when the Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IORD (PC Card Memory Mode)	I	44	This signal is not used in this mode.
-IORD (PC Card I/O Mode)		TTL Schmitt Trigger Input 100K Pull-Up	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-WE (PC Card Memory Mode)	I	15 TTL Schmitt Trigger Input 100K Pull-Up	This is a signal driven by the host and used for strobing memory write data to the registers of the Card Storage when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC.

SIGNAL DESCRIPTIONS

Signal Name	Dir	Pin	Description
-OE (PC Card Memory Mode)	I	9 TTL Schmitt Trigger Input	This is an Output Enable strobe generated by the host interface. It is used to read data from the Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-OE (True IDE Mode)			To enable True IDE Mode, this input should be grounded by the host.
RDY/-BSY (PC Card Memeory Mode)	O	16 TTL Tri-State 3mA Output	In Memory Mode, this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the Card is busy. The Host Memory Card Socket must provide a pull-up Resistor. At power up and at Reset, the RDY/-BSY signal is held low (Busy) until the PC Card has completed its power up or Reset function. No access of any type should be made to the Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			I/O Operation -- After the Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high Interrupt Request to the host.
A10-A0 (PC Card Memory Mode)	I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29 TTL Input	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the PC Card, the memory mapped port address registers within the PC Card, a byte in the card's information structure and its configuration control and status registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2-A0 (True IDE Mode)			In True IDE Mode only, HA (2:0) are used to select the one of eight registers in the Task File, the remaining address lines should be grounded.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 42 TTL Schmitt Trigger Input	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, and -CE2 allows 8 bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable		100K Pull-Up	This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.

SIGNAL DESCRIPTIONS

Signal Name	Dir	Pin	Description
-CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)		TTL Schmitt 100K Pull-Up	This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
-REG (PC Card Memory Mode) Attribute Memory Select	I	61 TTL Schmitt Trigger Input 100K Pull-Up	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC.
WP (PC Card Memory Mode) Write Protect	O	33	Memory Mode -- The Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)		TTL Tri-State 3mA Output	I/O Operation -- When the Card is configured for I/O Operation, Pin 33 is used for the "-I/O Selected" in 16 Bit Port (-IOIS16) function. A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode, this output signal is asserted low when this device is expecting a word data transfer cycle.
-INPACK (PC Card Memory Mode)	O	60	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge		TTL Tri-State 3mA Output	The Input Acknowledge signal is asserted by the Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the Card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
BVD1 (PC Card Memory Mode)	I/O	63	This signal is asserted high as the BVD1 signal since a battery is not used connected at the host.
-STSCHG (PC Card I/O Mode) Status Changed		TTL I/O 3mA Output 100K Pull-Up	This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.

SIGNAL DESCRIPTIONS

Signal Name	Dir	Pin	Description
-WAIT (PC Card Memeory Mode)	O	59 TTL Output 3mA Output	The -WAIT signal is driven low by the Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In the True IDE Mode, this output signal may be used as IORDY.
GND (PC Card Memeory Mode)	-	1, 34, 35, 68	Ground
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
VCC (PC Card Memory Mode)	-	17, 51	+5.0V or +3.3V power
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
RESET (PC Card Memory Mode)	I	58 TTL Input 100K Pull-Up	When the pin is high, this signal Resets the Card. The Card is Reset only at power up if this pin is left high or open from power-up. The Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as PC Card Memory Mode signal.
-RESET (True IDE Mode)			In True IDE Mode, this input pin is the active low hardware reset from the host.
-VS1 -VS2 (PC Card Memory Mode)	O	43	Voltage Sense Signals. -VS1 is groundedand -VS2 is not connected so that
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.

DC CHARACTERISTICS-1 (Ta= -65°C to +110°C, VCC=3.3V±5%. VDD=3.3V±5%)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Voltage (CMOS level)	VIHC VILC	0.7xVDD -0.3	—	VDD+0.3 0.2xVDD	V	
Input Voltage (TTL level)	VIHC VILC	2 -0.3	—	VCC+0.3 0.6	V	
Schmitt Circuit (CMOS level) 1	VTC+ VTC- VTC 2	-1.6 0.7 -0.3	— — —	2.6 (1.7) —	V V	VCC=3.3V
Output Voltage (CMOS) (1 mA) 3	VOH VOL	VDD-0.8 —	— —	— 0.4	V V	IOH=-0.5 mA IOL=1mA
Output Voltage (CMOS) (3 mA) 3	VOH VOL	VDD-0.8 —	— —	— 0.4	V V	IOH=-1 mA IOL=3mA
Output Voltage (TTL) (3 mA) 3	VOH VOL	VDD-0.8 —	— —	— 0.4	V V	IOH=-1 mA IOL=3mA
Output Voltage (TTL) (2 mA/3 mA) 3	VOH VOL	VDD-0.8 —	— —	— 0.4	V V	IOH=-2 mA IOL=3mA
Input Leakage Current 4	ILI	—	—	1	µA	
Output Leakage Current 4	ILO	—	—	1	µA	VOUT=High Impedance
Pull-up current/(Resistivity)	-IPU	5/(230)	80/(41)	230/(13.7)	µA/(kW)	VIN=GND
Pull-up current/(Resistivity) 5	-IPU	2/(1800)	16/(206)	36/(85)	µA/(kW)	VIN=GND
Sleep standby current 8	ISP1	—	(0.2)	(0.5)	mA	CMOS level (control signal=VCC-0.2)
Sector read current 6, 8	ICCR(DC) ICCR(Peak)	—	(25) (50)	(50) (80)	mA mA	CMOS level (control signal=VCC-0.2)
Sector write current 7, 8	ICCW(DC) ICCW(Peak)	—	(25) (50)	(50) (80)	mA mA	CMOS level (control signal=VCC-0.2)

DC CHARACTERISTICS-2 (Ta= -65°C to +110°C, VCC=5V±10%, VDD=3.3V±5%)9

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Voltage (CMOS level)	VIHC	0.7xVDD	—	VDD+0.3	V	
	VILC	-0.3	—	0.3xVDD	V	
Input Voltage (TTL level)	VIHC	2.4	—	VCC+0.3	V	
	VILC	-0.3	—	0.6	V	
Schmitt Circuit (CMOS level)1	VTC+	(2.8)		4.0	V	VCC=5V
	VTC-	1.1	—	(2.4)	V	
	VTC 2	(0.3)	—	—	V	
Output Voltage (CMOS)	VOH	VCC-0.8	—	—	V	IOH=-2 mA
(3 mA) 3	VOL	—	—	0.4	V	IOL=8 mA
Output Voltage (CMOS)	VOH	VCC-0.8	—	—	V	IOH=-6mA
(2 mA/3 mA) 3	VOL	—	—	0.4	V	IOL=8mA
Input Leakage Current 4	ILI	—	—	1	µA	
Output Leakage Current 4	ILO	—	—	1	µA	VOUT=High Impedance
Pull-up current/(Resistivity) 5	-IPU	10/(550)	45/(110)	90/(50)	µA/(kW)	VIN=GND
Sleep standby current 8	ISP1	—	(0.5)	(1.0)	mA	CMOS level
						(control signal=VCC-0.2)
Sector read current 6, 8	ICCR(DC)	—	(40)	(70)	mA	CMOS level
						(control signal=VCC-0.2)
	ICCR(Peak)		(80)	(120)	mA	
Sector write current 7, 8	ICCW(DC)	—	(45)	(75)	mA	CMOS level
						(control signal=VCC-0.2)
	ICCW(Peak)		(80)	(120)	mA	

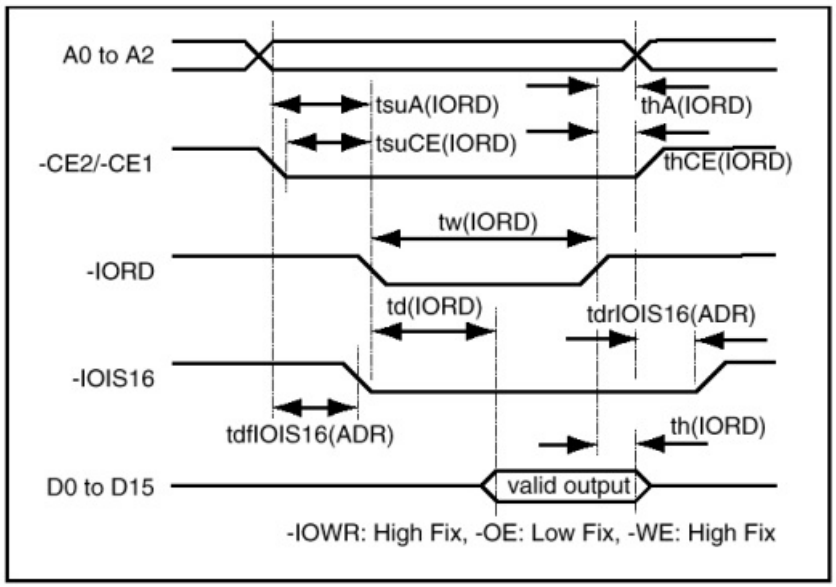
1. CMOS schmitt input is measured at V IH =V TC+max and V IL =V TC-min. ( ) is reference value.
2. V TC is reference value.
3. Measured for static state.
4. Except pulled up input/output pin.
5. Pull-up resister is 100 ký.
6. Measured during sector read transfer.
7. Measured during sector write transfer.
8. Power dissipation is reference value on the assembled flash card, including the flash memory.
9. Exept PC3O01C, PC3O03C, and PC3B43UC buffer type.
Refer to DC characteristics at VCC=3.3V

AC CHARACTERISTICS (Ta=Ta= -65°C to +110°C; VCC=5v±10% or VCC=3.3V±5%)

True IDE Mode Access Read AC Characteristics)

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

True IDE Mode Access Read Timing



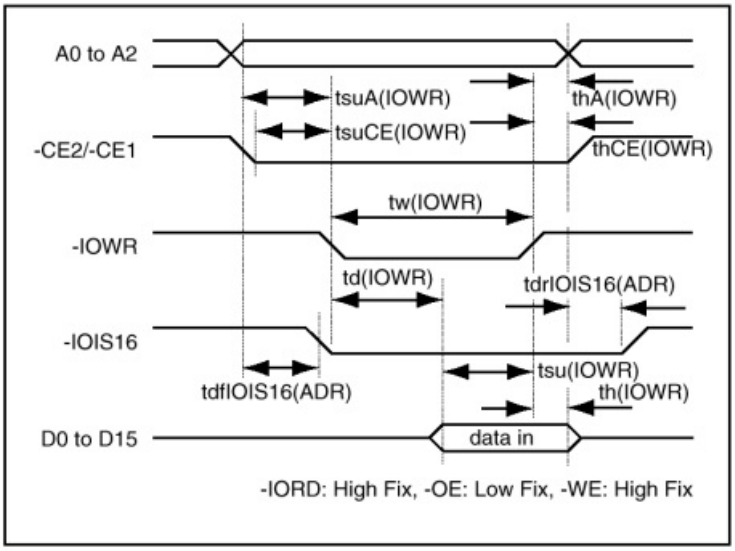
(Continued)

AC CHARACTERISTICS (continued)

True IDE Mode Access Write AC Characteristics

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH		100
Data Hold following IOWR	th(IOWR)	tIWHDX	0	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

True IDE Mode Access Write Timings

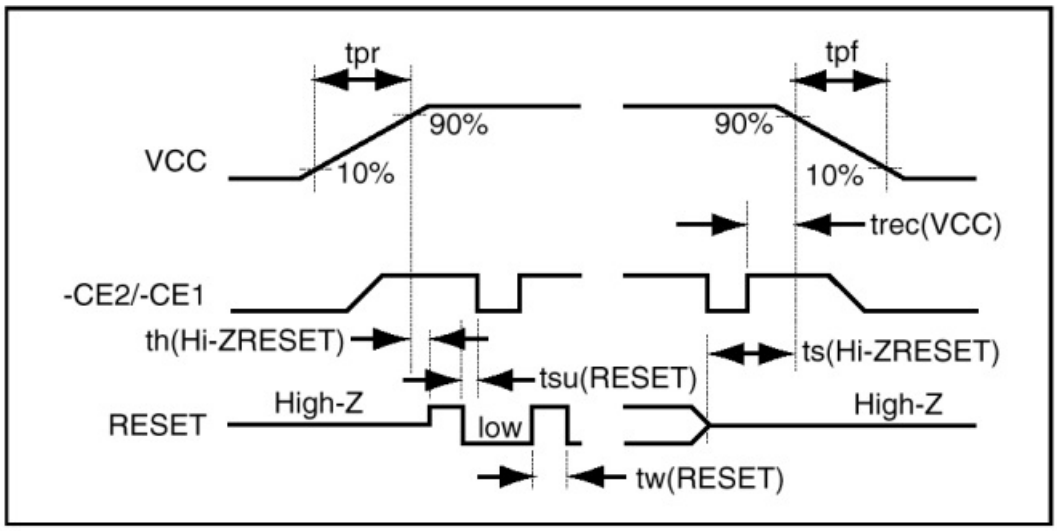


RESET CHARACTERISTICS

Hard Reset Characteristics

Item	Symbol	Min.	Max.	Unit
Reset Setup Time	tsu (RESET)	100		ms
-CE Recover Time	trec (VCC)	1		µs
VCC Rising Up Time	tpr	0.1	100	ms
VCC Falling Down Time	tpf	3	300	ms
Reset Pulse Width	tw (RESET)	10		µs
	th (Hi-ZRESET)	1		ms
	ts (Hi-ZRESET)	0		ms

Hard Reset Timings



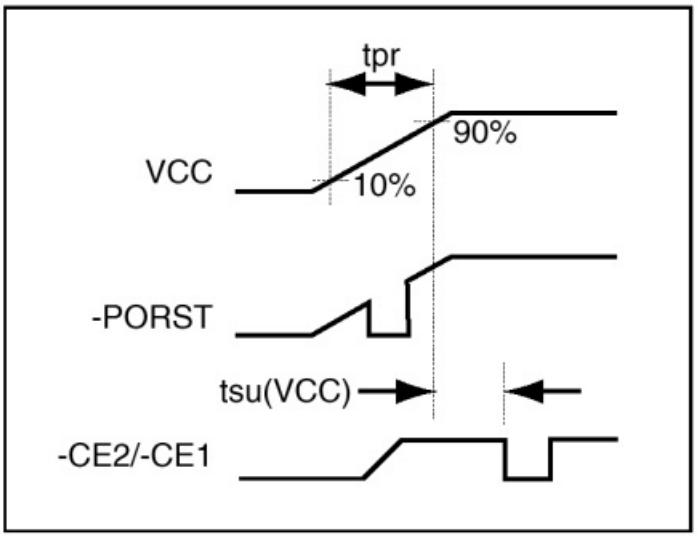
(continued)

RESET CHARACTERISTICS (continued

Power on Reset Characteristics

Item	Symbol	Min.	Max.	Unit
-CE Setup Time	tsu (VCC)	100		ms
VCC Rising Up Time	tpr	0.1	100	ms

Power on Reset Timings



TRUE IDE INTERFACE

The drive is configured in a True IDE mode of operation. Only I/O operation to the task file and data register are allowed. The drive is configured during power on sequence, is accessed in word (16-bit) mode at power on. The drive permits 8-bit accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

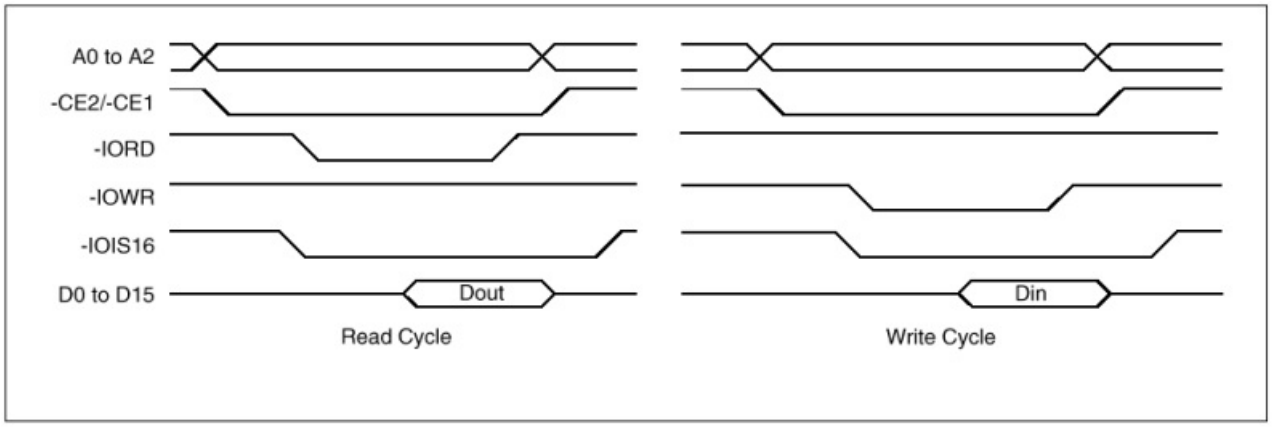
True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	x	x	x	High Z	High Z
Standby Mode	H	H	x	x	x	High Z	High Z
Data Register Access	H	L	0	L	H	Odd-Byte	Even-Byte
Alternate Status Access	L	H	6h	L	H	High Z	Status Out
Other Task File Access	H	L	1-7h	L	H	High Z	Data
x: L or H							

True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	x	x	x	Don't Care	Don't Care
Standby Mode	H	H	x	x	x	Don't Care	Don't Care
Data Register Access	H	L	0	H	L	Odd-Byte	Even-Byte
Control Register Access	L	H	6h	H	L	Don't Care	Control In
Other Task File Access	H	L	1-7h	H	L	Don't Care	Data
x: L or H							

True IDE Mode I/O Access Timing Example



TASK FILE REGISTER SPECIFICATION

These registers are used for reading and writing the storage data in this drive. The decoded addresses are shown as Follows.

True IDE Mode I/O Map

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector Count register	Sector Count register
1	0	0	1	1	Sector No. register	Sector No. register
1	0	1	0	0	Cylinder Low register	Cylinder Low register
1	0	1	0	1	Cylinder High register	Cylinder High register
1	0	1	1	0	Drive Head register	Drive Head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt Status register	Device Control register
0	1	1	1	1	Drive Address register	Reserved

Data Register

The Data Register is a 16 bit register that has read/write ability, and it is used for transferring 1 sector data between the drive and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

Error Register

This register is a read only register, and it is used for analyzing the error content at the drive accessing. This register is valid when the BSY bit in the Status register and Alternate Status register are set to "0" (Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

bit	Name	Function
7	BBK (Bad Block Detected)	This bit is set when a Bad Block is detected in requested ID field.
6	UNC (Data ECC Error)	This bit is set when Uncorrectable error is occurred at reading the drive.
4	IDNF (ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (ABoRTed Command)	This bit is set if the command has been aborted because of the drive status condition. (Not ready, Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

Feature Register

This register is a write only register and provides information regarding features of the drive which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature Byte							

Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the Drive. If the value in this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request. This register's initial value is “01h.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector Count Byte							

Sector Number Register

This register contains the starting sector number which is started by following the sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector Number Byte							

Cylinder Low Register

This register contains the low 8-bit of the starting cylinder address which is started by following sector transfer Command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder Low Byte							

Cylinder High Register

This register contains the high 8-bit of the starting cylinder address which is started by following sector transfer Command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder High Byte							

Drive/Head Register

This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DRV	Head No			

bit	Name	Function
7	1	This bit is set to “1”.
6	LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. In LBA mode. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00: Sector Number Register D7-D0 LBA15-LBA08: Cylinder Low Register D7-D0 LBA23-LBA16: Cylinder High Register D7-D0 LBA27-LBA24: Drive/Head Register bits HS3-HS0
5	1	This bit is set to “1”.
4	DRV (DRiVe select)	This bit is used for selecting the Master (Drive 0) and Slave (Drive 1) in Master/Slave organization. The drive is set to be Drive 0 or 1 by using DRV# of the Socket and Copy register.
3-0	Head Number (HS3-HS0)	These bits are used for selecting the Head number for the following command. Bit 3 is MSB.

Status Register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1, 2, 3) and level interrupt mode, -IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the drive internal operation is executing. When this bit is set to “1”, other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to “1”, the drive is capable of receiving the read and write or seek requests. If this bit is set to “0”, the drive prohibits these requests.
5	DWF (Drive Write Fault) .	This bit is set if this drive indicates the write fault status
4	DSC (Drive Seek Complete)	This bit is set when the drive seek is complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the drive receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to “0”.
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

Alternate Status Register

This register is the same as the Status register, so the bit assignment refers to previous item of the Status register. But this register is different from the Status register in that -IREQ is not negated when data read.

Command Register

This register is a write only register, and is used for writing the command that executes the drive operation. The command code written in the command register, after the parameter is written in the Task File during the drive Ready State.

Command	Code	FR	SC	SN	CY	DR	DH	LBA
Check Power Mode	E5h or 98h	N	N	N	N	Y	N	N
Execute Drive Diagnostic	90h	N	N	N	N	Y	N	N
Erase Sector	C0h	N	Y	Y	Y	Y	Y	Y
Format Track	50h	N	Y	N	Y	Y	Y	Y
Identify Drive	ECh	N	N	N	N	Y	N	N
Idle	E3h or 97h	N	Y	N	N	Y	N	N
Idle Immediate	E1h or 95h	N	N	N	N	Y	N	N
Initialize Drive Parameters	91h	N	Y	N	N	Y	Y	N
Read Buffer	E4h	N	N	N	N	Y	N	N
Read DMA	C8h	N	Y	Y	Y	Y	Y	Y
Read Multiple	C4h	N	Y	Y	Y	Y	Y	Y
Read Long Sector	22h or 23h	N	N	Y	Y	Y	Y	Y
Read Sector(s)	20h or 21h	N	Y	Y	Y	Y	Y	Y
Read Verify Sector(s)	40h or 41h	N	Y	Y	Y	Y	Y	Y
Recalibrate	1Xh	N	N	N	N	Y	N	N
Request Sense	03h	N	N	N	N	Y	N	N
Seek	7Xh	N	N	Y	Y	Y	Y	Y
Set Features	EFh	Y	N	N	N	Y	N	N
Set Multiple Mode	C6h	N	Y	N	N	Y	N	N
Set Sleep Mode	E6h or 99h	N	N	N	N	Y	N	N
Stand By	E2h or 96h	N	N	N	N	Y	N	N
Stand By Immediate	E0h or 94h	N	N	N	N	Y	N	N
Translate Sector	87h	N	Y	Y	Y	Y	Y	Y
Wear Level	F5h	N	N	N	N	Y	Y	N
Write Buffer	E8h	N	N	N	N	Y	N	N
Write DMA	CAh	N	Y	Y	Y	Y	Y	Y
Write Long Sector	32h or 33h	N	N	Y	Y	Y	Y	Y
Write Multiple	C5h	N	Y	Y	Y	Y	Y	Y
Write Multiple w/o Erase	CDh	N	Y	Y	Y	Y	Y	Y
Write Sector(s)	30h or 31h	N	Y	Y	Y	Y	Y	Y
Write Sector(s) w/o Erase	38h	N	Y	Y	Y	Y	Y	Y
Write Verify	3Ch	N	Y	Y	Y	Y	Y	Y

FR=Feature Register
SC=Sector CountRegister
SN=Sector Number Register
CY=Cylinder Registers
DR=DRV bit of Drive/Head Register
DH=Head Number of Drive/Head Register,
LBA=Logical Block Address Mode Supported.

Y --The register contains a valid parameter for this command.
N --The register does not contain a valid parameter for this command.

Device Control Register

This register is a write only register, and is used forcontrolling the drive interrupt request and issuing an ATA soft reset to the drive.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	1	SRST	nIEN	0

bit	Name	Function
7-4	x	Don't care.
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the drive to perform Task File Reset operation. This does not change the Drive Configuration registers as a Hardware Reset does. The drive remains in Reset until this bit is reset to "0".
1	nIEN (Interrupt ENable)	This bit is used for enabling -IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

Drive Address Register

This register is a read only register, and it is used for confirming the drive status. This register is provided for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit 7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7	x	This bit is unknown.
6	nWTG (WriTing Gate)	This bit is unknown.
5-2	nHS3-0 (Head Select 3-0)	These bits is the negative value of the Head Select bits (bit 3 to 0) in the Drive/Head register
1	nDS1 (Drive Select 1)	This bit is unknown.
0	nDS0 (Drive Select 0)	This bit is unknown.

ATA COMMAND SPECIFICATIONS

This table with the following paragraphs summarizes the ATA command set and shows the support commands and thecommand codes which are written in the command registers.

Number	Command	Code	FR	SC	SN	CY	DR	DH	LBA
1	Check Power Mode	E5h or 98h	N	N	N	N	Y	N	N
2	Execute Drive Diagnostic	90h	N	N	N	N	Y	N	N
3	Erase Sector	C0h	N	Y	Y	Y	Y	Y	Y
4	Format Track	50h	N	Y	N	Y	Y	Y	Y
5	Identify Drive	ECh	N	N	N	N	Y	N	N
6	Idle	E3h or 97h	N	Y	N	N	Y	N	N
7	Idle Immediate	E1h or 95h	N	N	N	N	Y	N	N
8	Initialize Drive Parameters	91h	N	Y	N	N	Y	Y	N
9	Read Buffer	E4h	N	N	N	N	Y	N	N
10	Read DMA	C8h	N	Y	Y	Y	Y	Y	Y
11	Read Multiple	C4h	N	Y	Y	Y	Y	Y	Y
12	Read Long Sector	22h or 23h	N	N	Y	Y	Y	Y	Y
13	Read Sector(s)	20h or 21h	N	Y	Y	Y	Y	Y	Y
14	Read Verify Sector(s)	40h or 41h	N	Y	Y	Y	Y	Y	Y
15	Recalibrate	1Xh	N	N	N	N	Y	N	N
16	Request Sense	03h	N	N	N	N	Y	N	N
17	Seek	7Xh	N	N	Y	Y	Y	Y	Y
18	Set Features	EFh	Y	N	N	N	Y	N	N
19	Set Multiple Mode	C6h	N	Y	N	N	Y	N	N
20	Set Sleep Mode	E6h or 99h	N	N	N	N	Y	N	N
21	Stand By	E2h or 96h	N	N	N	N	Y	N	N
22	Stand By Immediate	E0h or 94h	N	N	N	N	Y	N	N
23	Translate Sector	87h	N	Y	Y	Y	Y	Y	Y
24	Wear Level	F5h	N	N	N	N	Y	Y	N
25	Write Buffer	E8h	N	N	N	N	Y	N	N
26	Write DMA	CAh	N	Y	Y	Y	Y	Y	Y
27	Write Long Sector	32h or 33h	N	N	Y	Y	Y	Y	Y
28	Write Multiple	C5h	N	Y	Y	Y	Y	Y	Y
29	Write Multiple w/o Erase	CDh	N	Y	Y	Y	Y	Y	Y
30	Write Sector(s)	30h or 31h	N	Y	Y	Y	Y	Y	Y
31	Write Sector(s) w/o Erase	38h	N	Y	Y	Y	Y	Y	Y
32	Write Verify	3Ch	N	Y	Y	Y	Y	Y	Y

FR=Features Register
SC=Sector Count Register (00h to FFh)
SN=Sector Number Register (01h to 20h)
CY=Cylinder Registers
DR=Drive bit of Drive/Head Register
HD=Head no. (0 to 3) of Drive/Head Register
LBA=Logical Block Address Mode

Y --Set up.
"--" -- Not set up.

Check Power Mode
(code: E5h or 98h)
This command checks the power mode.

Execute Drive Diagnostic
(code: 90h)
This command performs the internal diagnostic tests implemented by the drive.

Erase Sector(s)
(code: C0h)
This command is used to erase data sectors.

Format Track
(code: 50h)
This command writes the desired head and cylinder of the selected drive. But selected sector data is not changed. This card accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command.

Identify Drive
(code: ECh)
This command enables the host to receive parameter Information from the drive.

Identify Drive Information

Word Address	Data	Total Bytes	Description
0	848AH	2	General configuration bit-significant information
1	XXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformmatted bytes per track
5	XXXXH	2	Number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7-8	XXXXH	4	Number of sectors per card (word7=MSW, word 8 = LSW)
9	0000H	2	Reserved
10-19	XXXXH	20	Reserved
20	0002H	2	Buffer type (dual ported, multi-sector, with read cache)
21	0002H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long commands
23-46	XXXXH	48	Firmware revision in ASCII
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT supported (bit 8), LBA supported (bit 9)
50	0000H	2	Reserved
51	0100H	2	PIO data transfer cycle timing mode 1
52	0000H	2	DMA data transfer cycle timing mode not supported
53-58	XXXXH	12	Reserved
59	010XH	2	Multiple sector setting is valid
60-61	XXXXH	4	Total number of sectors addressable in LBA Mode
62-255	0000H	388	Reserved

XXXXH: These values are dependent upon the the specific card.

Idle
(code: E3h or 97h)
This command causes the drive to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

Idle Immediate
(code: E1h or 95h)
This command causes the drive to set BSY, enter the Idle (Read) mode, clear BSY, and generate an interrupt.

Initialize Drive Parameters
(code: 91h)
This command enables the host to set the number of sectors per track and the number of heads per cylinder.

Read Buffer
(code: E4h)
This command enables the host to read the current contents of the drive's sector buffer.

Read Multiple
(code: C4h)
This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Read Long Sector
(code: 22h or 23h)
This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

Read Sector(s)
(code: 20h or 21h)
This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified tin the Sector Number register.

Read Verify Sector(s)
(code: 40h or 41h)
This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to theHost.

Recalibrate
(code: 1Xh)
This command is effectively a NOP command to the driveand is provided for compatibility purposes.

Request Sense
(Code: 03h)
This command requests an extended error code after command ends with an error.

Seek
(code: 7Xh)
This command is effectively a NOP command to the drivealthough it does perform a range check.

Set Features
(code: EFh)
This command is used by the host to establish or select certain features

Feature	Description
01H	Enable 8-bit data transfers
55H	Disable Read Look Ahead
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset
81H	Disable 8-bit data transfers
BBH	4bytes of data apply on Read/Write Long commands
CCH	Enable Power on Reset (POR) establishment of default at Soft Reset

Set Multiple Mode
(code: C6h)
This command enables the drive to perform Read and Write Multiple operations and establishes the block count for these Commands.

Set Sleep Mode
(code: E6h or 99h)
This command causes the drive to set BSY, enter the Sleep mode, clear BSY, and generate an interrupt.

Stand By
(code: E2h or 96h)
This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY, and return the interrupt immediately.

Stand By Immediate
(code: E0h or 94h)
This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

Translate Sector
(code: 87h)
This command allows the host a method of derermining the exact number of times a user sector has been erased and Programmed.

Wear Level
(code: F5h)
This command effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.

Write Buffer
(code: E8h)
This command enables the host to overwrite contents of the drive's sector buffer with any data pattern desired.

Write Long Sector
(code: 32h or 33h)
This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

Write Multiple
(code: C5h)
This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

Write Multiple without Erase
(Code: CDh)
This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.

Write Sector(s)
(code: 30h or 31h)
This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

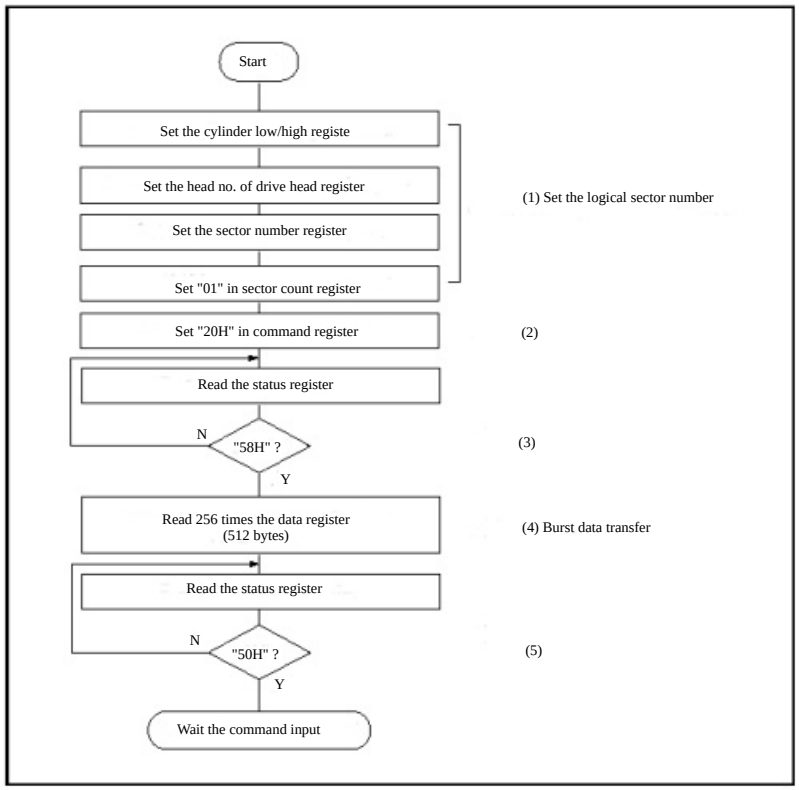
Write Sector(s) without Erase
(code: 38h)
This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

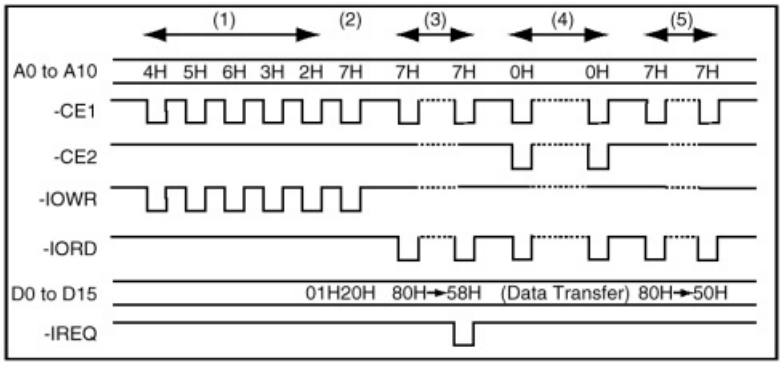
Write Verify
(code: 3Ch)
This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

SECTOR TRANSFER PROTOCOL

Sector Read

One sector read procedure is shown in the following charts.





Sector Write

One sector write procedure is shown in the following charts.